Control Circuit Templates for Asynchronous Bundled-Data Pipelines

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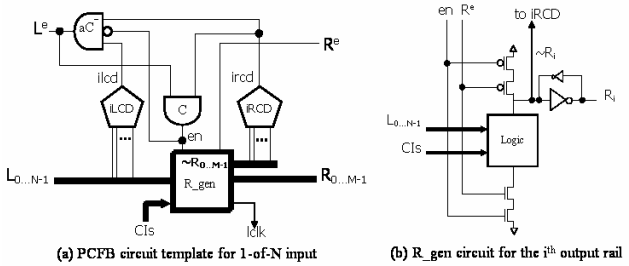
Abstract

This paper proposes the use of templatized asynchronous control circuits with single-rail datapaths to create low-power bundled-data non-linear pipelines. First, we adapt an existing templatized control style for 1-of-N rail pipelines, the Pre-Charged Full Buffer PCFB [1], to bundled-data pipelines. Then, we present a novel true 4-phase template (T4PFB) that has lower control overhead. Simulation results indicate 12%-44% higher throughput for the pipeline stage equivalent to 8 to 40 gates.

Asynchronous bundled-data pipelines can often achieve low power and high average-case performance [2]. They use mature synchronous standard-cell datapath design coupled with a matched delay line and asynchronous circuits to control request-acknowledge handshaking. For complex systems, the design of these controls is difficult and error-prone. To simplify this control circuit design, this paper proposes to adopt and extend 1-of-N rail circuit templates. That is, pipeline stages communicate with 1-of-N rail control information coupled with single-rail data.



(a) PCFB circuit template for 1-of-N input and 1-of-M output channels

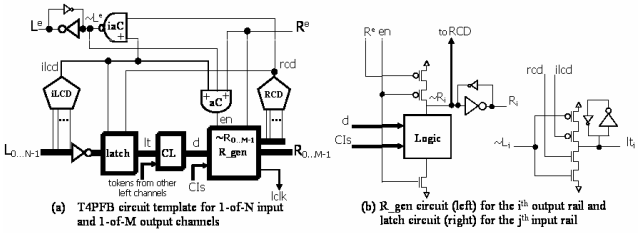
(b) R_gen circuit for the i^{th} output rail

Fig. 1 PCFB template and a detailed circuit.

The modified PCFB template for 1-of-N control of bundled-data pipelines (Fig. 1) has one R_gen block for each output rail (*Ri*). It is different from the original PCFB in that the conditional inputs (CIs) may have single-rail encoding and that the local clock signal(s) *lclk(s)* has no associated acknowledgement. The local clock signal is implemented either as a distinct *Ri* output or a combinational function of other *Ri's*. The iLCD and iRCD blocks are inverting left and right completion detectors [1].

The original PCFB template is robust because there are no internal timing assumptions on gate delays, i.e., it is quasi-delay-insensitive. Our adaptations, however, has setup and hold constraints on the conditional inputs typical of bundled-data designs.

The major drawback of the PCFB template is that the control overhead is large because the set phase of the delay line alone must be matched to the worst-case delay of the datapath. This means that the reset delay of the delay line represents control overhead that hinders performance. To minimize this control overhead, more complex *asymmetric* delay lines are necessary. Lastly, the combinational logic necessary to determine *R* outputs is limited to what can be implemented in a single R_gen gate.



(a) T4PFB circuit template for 1-of-N input and 1-of-M output channels

(b) R_gen circuit (left) for the i^{th} output rail and latch circuit (right) for the j^{th} input rail

Fig. 2 T4PFB template and a detailed circuit.

To address these limitations, we designed a new circuit template that follows the true 4-phase handshaking protocol. In particular, our template (Fig. 2) differs from PCFB template in that the matched delay includes both phases of the delay line, significantly reducing control overhead. Consequently, the control overhead of T4PFB is independent of the length of the delay line, facilitating the use of smaller and lower power symmetric delay lines. In addition, HSPICE simulation results in a 0.25µ process demonstrated that compared to the PCFB template, the T4PFB template achieves between 12% and 44% higher throughput for identical datapaths with delay between 8 and 40 gates [3].

[1] A. Lines, *Pipeline Asynchronous Circuits*, M.S. thesis, California Institute of Technology, 1998.

[2] C. H. van Berkel, M. B. Josephs, and S. M. Nowick. Scanning the technology: Applications of asynchronous circuits. *Proceedings of the IEEE*, 87(2):223-233, Feb. 1999.

[3] S. Tugsinavisut and P.A. Beerel, Control circuit templates for asynchronous bundled-data pipelines. Technical Report CENG 01-06, EE-Systems, USC, December 2001.